What is claimed is:

1. An integrated circuit device, comprising:

a data inversion circuit that is configured to evaluate bit differences between first and second ordered groups of data received in parallel at inputs thereof by performing bit-to-bit comparisons between corresponding bits in the first and second ordered groups of data and is further configured to generate versions of the first and second ordered groups of data in parallel at outputs thereof, wherein the version of the second ordered group of data is an inverted version of the second ordered group of data when a number of bit differences between the version of the first ordered group of data and the second ordered group of data is greater than one-half the number of bits of data within the second ordered group of data, said data inversion circuit comprising an XOR circuit that is configured to receive the first and second ordered groups of data, a comparator that is configured to generate a first internal parity signal in response to signals generated by said XOR circuit and a parity signal generator that is configured to generate a second external parity signal in response to a first external parity signal and the first internal parity signal signal.

2. The device of Claim 1, wherein the first external parity signal identifies whether the version of the first ordered group of data is an inverted or noninverted version of the first ordered group of data and the second external parity signal identifies whether the version of the second ordered group of data is an inverted or noninverted version of the second ordered group of data.

3. The device of Claim 1, wherein said comparator is configured to generate a pair of complementary internal parity signals in response to signals generated by said first XOR circuit.

4. The device of Claim 1, wherein said parity signal generator is configured to generate a pair of complementary internal parity signals in response to the first internal parity signal.

5. The device of Claim 3, wherein said parity signal generator is configured to select a first one of the pair of complementary internal parity signals as the second external parity signal when the first externalparity signal is in a first logic state and is further configured to select a second one of the pair of complementary internal parity signals as the second external parity signal when the first external parity signal is in a second logic state opposite the first logic state.

6. An integrated circuit device, comprising:

a data inversion circuit that is configured to evaluate bit differences between first and second ordered groups of data received in parallel at inputs thereof by performing bit-to-bit comparisons between corresponding bits in the first and second ordered groups of data and is further configured to generate a version of the first ordered group of data in parallel with an inverted version of the second ordered group of data at outputs thereof when a number of bit differences between the version of the first ordered group of data and the second ordered group of data is greater than one-half the number of bits of data within the second ordered group of data, said data inversion circuit comprising a plurality of parity signal generators that are configured to generate at least a first external parity signal that identifies whether the version of the first ordered group of data is an inverted or noninverted version of the first ordered group of data.

7. The device of Claim 5, wherein said data inversion circuit comprises at least one delay circuit that is configured to generate a delayed version of the first ordered group of data in response to the first ordered group of data and is further configured to generate the version of the first ordered group of data at an output of said data inversion circuit in response to the delayed version of the first ordered group of data and the first external parity signal.

8. The device of Claim 6, wherein a delay provided by the at least one delay circuit is of sufficient duration to maintain a delay margin between a

leading edge of the at least a first external parity signal and corresponding leading edges of the data in the delayed version of the first ordered group of data, within a threshold delay margin.

9. A data inversion circuit of a semiconductor device with a multiple bit pre-fetch structure, the data inversion circuit comprising:

a plurality of inversion circuits that in parallel receive a plurality of input data pre-fetched simultaneously with initial input data, perform inversion/non-inversion of the plurality of input data, and generate a plurality of output data,

wherein the initial input data is output data output during a previous clock cycle and each of the plurality of inversion circuits receives two input data neighboring in an output order among the initial input data and the plurality of input data, determines how many of corresponding bits of the two input data are toggled to each other, and performs inversion/non-inversion for latter one of the two input data according to the determination of how many of the corresponding bits of the two input data are toggled.

10. The data inversion circuit of claim 9, wherein each of the initial input data and the plurality of input data includes I bits and the output order is an order when the plurality of input data is output to an external source through I data output pads of the semiconductor device after the plurality of input data are subjected to inversion/non-inversion by the plurality of inversion circuits, where I is a positive integer greater than one.

11. The data inversion circuit of claim 10, wherein at least one of the plurality of inversion circuits comprises:

a first logic circuit, which receives the initial input data and first input data among the plurality of input data, determines a result of how many bits of the initial input data are toggled with corresponding bits of the first input data, and outputs an internal logic signal according to the determined result;

a comparator, which outputs a flag signal in response to the internal logic signal; and

a second logic circuit, which inverts and outputs the first input data or outputs the first input data without inversion, as first output data of the plurality of output data, in response to the flag signal.

12. The data inversion circuit of claim 11, wherein the internal logic signal includes the I bits, and the first logic circuit outputs a same number of bits as the number of toggled bits of the initial input data and the first input data among the I bits of the internal logic signal, in a first level.

13. The data inversion circuit of claim 12, wherein the comparator outputs a flag signal at a first logic level if half or more of the I bits of the internal logic signal are bits with the first logic level and outputs a flag signal at a second logic level, opposite the first logic level, if less than half of the I bits of the internal logic signal are bits with the first logic level; and

the second logic circuit inverts the first input data and outputs the inverted result as the first output data if the flag signal is at the first logic level, and outputs the first input data without inversion as the first output data if the flag signal is at the second logic level.

14. The data inversion circuit of claim 11, wherein the comparator comprises:

a comparison voltage generator circuit, which generates a comparison voltage in response to the internal logic signals;

a reference voltage generator circuit, which generates a predetermined reference voltage;

a differential amplifier, which compares the comparison voltage with the reference voltage and outputs the flag signal according to the compared result.

15. The data inversion circuit of claim 11, wherein at least one of the plurality of inversion circuits further includes a delay circuit which receives the first input data, delays the first input data by a predetermined time, and outputs the delayed first input data to the second logic circuit, wherein the

predetermined time is a time taken until the flag signal is output from the comparator after the first input data is input to the first logic circuit.

16. The data inversion circuit of claim 10, wherein at least one of the plurality of inversion circuits comprises:

a first logic circuit, which receives Jth input data and Jth-1 input data among the plurality of input data, determines a result of how many bits of the Jth input data are toggled with corresponding bits of the Jth-1 input data, and outputs an internal logic signal according to the determined result, where J is a positive integer greater than one;

a comparator, which outputs an internal flag signal in response to the internal logic signal;

a flag signal generator circuit, which inverts and outputs the internal flag signal or outputs the internal flag signal without inversion, as a Jth flag signal, in response to a Jth-1 flag signal; and

a second logic circuit, which inverts and outputs the Jth input data among the plurality of output data or outputs the Jth input data without inversion, as Jth output data, in response to the Jth flag signal.

17. The data inversion circuit of claim 16, wherein the internal logic signal includes the I bits, and the first logic circuit outputs a same number of bits as the number of toggled bits of the Jth input data and the Jth-1 input data among the I bits of the internal logic signal, in a first logic level.

18. The data inversion circuit of claim 17, wherein the comparator outputs the internal flag signal at the first logic level if half or more of the I bits of the internal logic signal are bits at the first logic level and outputs the internal flag signal with a second logic level if less than half of the I bits of the internal logic signal are bits with the first logic level,

the flag signal generator inverts and outputs the internal flag signal as the Jth flag signal if the Jth-1 flag signal is in the first logic level, and outputs the internal flag signal without inversion as the Jth flag signal if the Jth-1 flag signal is in the second logic level, and

the second logic circuit inverts and outputs the Jth input data as the Jth output data if the Jth flag signal is in the first logic level, and outputs the Jth input data without inversion as the Jth output data if the Jth flag signal is in the second logic level.

19. The data inversion circuit of claim 17, wherein the comparator comprises:

a comparison voltage generator circuit, which generates a comparison voltage in response to the internal logic signals;

a reference voltage generator circuit, which generates a predetermined reference voltage; and

a differential amplifier which compares the comparison voltage with the reference voltage and outputs the internal flag signal according to the compared result,

wherein a level of the comparison voltage is higher than a level of the reference voltage if half or more among the I bits of the internal logic signal are bits with the first logic level.

20. The data inversion circuit of claim 16, wherein the flag signal generator comprises:

a first inverter, which inverts the internal flag signal and outputs the inverted internal flag signal;

a second inverter, which inverts the Jth flag signal and outputs the inverted Jth flag signal;

a first switch, which is turned on or off in response to the Jth flag signal, receives the inverted internal flag signal when the first switch is turned on, and outputs the inverted internal flag signal; and

a second switch, which is turned on or off in response to the inverted Jth flag signal, receives the internal flag signal when the second switch is turned on, and outputs the internal flag signal.

21. The data inversion circuit of claim 16, wherein at least one of the plurality of inversion circuits further comprises a delay circuit which receives

the Jth input data, delays the Jth input data by a predetermined time, and outputs the delayed Jth input data to the second logic circuit,

wherein the predetermined time is a time taken until the Jth flag signal is output from the flag signal generator after the Jth input data is input to the first logic circuit.

22. The data inversion circuit of claim 10, wherein at least one of the plurality of inversion circuits comprises:

a first logic circuit, which receives Jth input data and Jth-1 input data among the plurality of input data, determines a result of how many bits of the Jth input data are toggled with corresponding bits of the Jth-1 input data, and outputs an internal logic signal according to the determined result, where J is a positive integer greater than one;

a comparison circuit, which outputs an internal flag signal and an inverted internal flag signal in response to the internal logic signal;

a selector, which selects any one of the internal flag signal and the inverted internal flag signal in response to a Jth-1 flag signal and outputs the selected signal as a Jth flag signal; and

a second logic circuit, which inverts and outputs the Jth input data or outputs the Jth input data without inversion, as Jth output data among the plurality of output data, in response to the Jth flag signal.

23. The data inversion circuit of claim 22, wherein the internal logic signal includes the I bits, and the first logic circuit outputs a same number of bits as the number of toggled bits of the Jth input data and the Jth-1 input data among the I bits of the internal logic signal, in a first logic level.

24. The data inversion circuit of claim 23, wherein the comparison circuit outputs an internal flag signal with the first logic level and an inverted internal flag signal with a second logic level if half or more among the I bits of the internal logic signal are bits with the first logic level, and outputs an internal flag signal with the second logic level and an inverted internal flag signal with the first logic level if less than half among the I bits of the internal logic signal are bits with the first logic level,

the selector outputs the inverted internal flag signal as the Jth flag signal if the Jth-1 flag signal is in the first logic level and outputs the internal flag signal as the Jth flag signal if the Jth-1 flag signal is in the second logic level, and

the second logic circuit inverts and outputs the Jth input data if the Jth flag signal is in the first logic level and outputs the Jth input data without inversion, as the Jth output data, if the Jth flag signal is in the second logic level.

25. The data inversion circuit of claim 23, wherein the comparison circuit comprises:

a comparator, which outputs the internal flag signal in response to the internal logic signals; and

an inverter, which inverts the internal flag signal and outputs the inverted internal flag signal,

wherein the comparator comprises:

a comparison voltage generator circuit, which generates a comparison voltage in response to the internal logic signals;

a reference voltage generator circuit, which generates a predetermined reference voltage; and

a differential amplifier, which compares the comparison voltage with the reference voltage and outputs the internal flag signal according to the compared result,

wherein the comparison voltage is larger than the reference voltage if half or more of the I bits of the internal logic signal are bits with the first logic level.

26. The data inversion circuit of claim 23, wherein the comparison circuit comprises:

a comparison voltage generator circuit, which generates a comparison voltage in response to the internal logic signals;

a reference voltage generator circuit, which generates a predetermined reference voltage; and

an internal flag signal generator circuit, which compares the comparison voltage with the reference voltage and outputs the internal flag signal and the inverted internal flag signal according to the compared result,

wherein a level of the comparison voltage is higher than the reference voltage if half or more of the I bits of the internal logic signal are bits with the first logic level.

27. The data inversion circuit of claim 26, wherein the internal flag signal generator circuit comprises:

a differential amplifier circuit, which is enabled or disabled in response to a control signal, compares the comparison voltage with the reference voltage when enabled, and outputs a first output signal to a first node and outputs a second output signal to a second node according to the compared result;

a first output circuit, which receives the first output signal output from the first node in response to the control signal and outputs the received first output signal as the internal flag signal; and

a second output circuit, which receives the second output signal output from the second node in response to the control signal and outputs the received second output signal as the inverted internal flag signal.

28. The data inversion circuit of claim 27, wherein the differential amplifier circuit comprises:

a current source circuit, which is enabled or disabled in response to the control signal;

differential transistors, which change a level of one of the first output signal and the second output signal and output the changed result to a first output line pair in response to the comparison voltage and the reference voltage when the current source circuit is enabled;

amplifier transistors, which amplify the first output signal and the second output signal on the first output line pair when the current source circuit is enabled, and outputs the amplified signals to a first node and a second node of a second output line pair, respectively; and

reset transistors, which are turned on or off in response to the control signal and precharge the first output line pair and the second output line pair to an internal voltage level when the reset transistors are turned on.

29. The data inversion circuit of claim 28, wherein the amplifier transistors are cross-coupled with the second output line pair.

30. The data inversion circuit of claim 28, wherein the first output circuit comprises:

a first inverter circuit, which is enabled or disabled in response to the control signal and inverts and outputs the first output signal output from the first node when the first inverter circuit is enabled; and

a first latch circuit, which latches an inverted first output signal output from the first inverter circuit and inverts and outputs the latched signal as the internal flag signal,

wherein the second output circuit comprises:

a second inverter circuit, which is enabled or disabled in response to the control signal and inverts and outputs the second output signal output from the second node when the second inverter circuit is enabled; and

a second latch circuit, which latches an inverted second output signal output from the second inverter circuit and inverts and outputs the latched signal as the inverted internal flag signal,

wherein the first inverter circuit and the second inverter circuit are disabled when the reset transistors are turned on.

31. The data inversion circuit of claim 22, wherein the selector comprises:

an inverter, which inverts the Jth flag signal and outputs the inverted Jth flag signal;

a first switch, which is turned on or off in response to the Jth flag signal and receives and outputs the inverted internal flag signal when the first switch is turned on; and

a second switch, which is turned on or off in response to the inverted Jth flag signal and receives and outputs the internal flag signal when the second switch is turned on.

32. The data inversion circuit of claim 22, wherein at least one of the plurality of inversion circuits further comprises a delay circuit which receives the Jth input data, delays the Jth input data by a predetermined time, and outputs the delayed Jth input data to the second logic circuit,

wherein the predetermined time is a time taken until the Jth flag signal is output from the selector after the Jth input data is input to the first logic circuit.

33. A data inversion method used in a semiconductor device with a multiple bit pre-fetch structure, the method comprising:

(a) in parallel receiving a plurality of input data simultaneously pre-fetched with initial input data;

(b) determining how many of corresponding bits of two input data neighboring in an output order among the initial input data and the plurality of input data are toggled to each other and generating a plurality of flag signals according to the determined result; and

(c) performing inversion/non-inversion of the plurality of input data in response to the plurality of flag signals and generating a plurality of output data,

wherein the initial input data is output data output during a previous clock cycle.